What is claimed is:

1. A distributed memory switch system for transmitting packets from source ports to destination ports, comprising:

a plurality of ports including a source port and a destination port wherein a packet is transmitted from the source port to the destination port;

a memory pool; and

an interconnection stage coupled between the plurality of ports and the memory pool such that the interconnection stage permits a packet to be sent from the source port to the destination port via the memory pool.

2. The distributed memory switch system of claim 1 wherein the interconnection stage comprises a switch stage connected to the plurality of ports.

3. The distributed memory switch system of claim 2 wherein the switch stage comprises a first set of ASICs connected to the plurality of ports.

4. The distributed memory switch system of claim 2 wherein the switch stage comprises at least one ASIC connected to the plurality of ports.

5. The distributed memory switch system of claim 2 wherein the switch stage comprises at least four ASICs connected to the plurality of ports.

6. The distributed memory switch system of claim 2 wherein the switch stage determines addresses in the memory pool for storing the packets received from the source ports.

7. The distributed memory switch system of claim 2 wherein the switch stage distributes packets received from the source ports into packet portions.

8. The distributed memory switch system of claim 2 wherein the switch stage reconstructs packet portions retrieved from the memory pool into a packet associated with the packet portions.

9. The distributed memory switch system of claim 2 wherein the switch stage forms command signals which are associated with packets received from the source ports.

10. The distributed memory switch system of claim 2 wherein the interconnection stage further comprises a memory switch connected to the switch stage and to the memory pool.

11. The distributed memory switch system of claim 10 wherein the memory switch comprises a second set of ASICs connected to the switch stage and to the memory pool.

12. The distributed memory switch system of claim 10 wherein the memory switch comprises at least four ASICs connected to the switch stage and to the memory pool.

13. The distributed memory switch system of claim 1 further comprising:

a switch engine coupled to the interconnection stage for managing the flow of packets between source ports and destination ports.

14. The distributed memory switch system of claim 13 further comprising:

a table RAM coupled to the switch engine.

15. A switch system for switching packets between ports, comprising:

an interconnection stage configured to transmit packets between ports; and

a memory pool coupled to the interconnection stage for storing packets which are received from the ports.

16. The switch system of claim 15 wherein the interconnection stage comprises a switch stage connected to the ports.

17. The switch system of claim 16 wherein the switch stage comprises a first set of integrated circuits connected to the ports.

18. The switch system of claim 16 wherein the switch stage comprises at least one integrated circuit connected to the ports.

19. The switch system of claim 16 wherein the switch stage comprises at least four integrated circuits connected to the ports.

20. The memory switch system of claim 16 wherein the switch stage determines addresses in the memory pool for storing the packets received from the ports.

21. The switch system of claim 16 wherein the switch stage distributes packets received from the ports into packet portions.

22. The switch system of claim 16 wherein the switch stage reconstructs packet portions retrieved from the memory pool into a packet associated with the packet portions.

23. The switch system of claim 16 wherein the switch stage forms command signals which are associated with packets received from the ports.

24. The switch system of claim 16 wherein the interconnection stage further comprises a memory switch connected to the switch stage and to the memory pool.

25. The switch system of claim 24 wherein the memory switch comprises a second set of integrated circuits connected to the switch stage and to the memory pool.

26. The switch system of claim 24 wherein the memory switch comprises at least four integrated circuits connected to the switch stage and to the memory pool.

27. The switch system of claim 15 further comprising:

a switch engine coupled to the interconnection stage for managing the flow of packets between the ports.

28. The switch system of claim 27 further comprising:

a table RAM coupled to the switch engine.

29. A method for transmitting packets from source ports to destination ports, comprising the steps of:

(a) detecting the arrival of a packet from a source port;

(b) determining the address locations in a memory pool for buffering the arrived packet after the packet is received from the source port of the packet;

(c) buffering the arrived packet in the memory pool after the packet is received from the source port;

(d) retrieving the packet in the memory pool; and

(e) transmitting the packet from the memory pool to the destination port of the packet.

30. The method of claim 29 further comprising the step of:

(f) prior to the buffering step (c), distributing the packet into packet portions.

31. The method of claim 30 further comprising the step of:

(g) after the retrieving step (d), reconstructing the packet portions into the packet.

32. The method of claim 30 further comprising the step of:

(g) prior to the retrieving step (d), obtaining the addresses of the memory pool which buffer the packet portions.

33. The method of claim 29 further comprising the step of:

(f) prior to the buffering step (c), forming a command signal for the packet from the source port.